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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/739,350	12/19/2003	Carl Taussig	200312389-1	1352

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EXAMINER	
NGUYEN, TAN	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/739,350	TAUSSIG ET AL.	
	Examiner	Art Unit	
	Tan T. Nguyen	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,8,9,12,13,19,20,22,25 and 27* is/are rejected.

7)☒ Claim(s) *5-7, 10-11, 14-18, 21, 23-24, 26, 28, 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The Information Disclosure Statement submitted on December 19, 2003 has been received and fully considered.

2. The drawings are objected to because in Figure 7, the nodes –104--, --106-- , the voltages –A--, --B--, --C-- should be inserted. Also, the reference number "114" for the column address diodes should be changed to –124-- . Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4, 8-9, 12-13, 19, 20, 22, 25, 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Taussig et al. (U.S. Patent No. 6,385,075).

Regarding claims 1, Taussig et al. disclosed in Figure 7 an address circuitry for a cross-point memory array comprising a first set of cross point row address diodes [114] (column 10, line 21) connected to a first set of address lines (unnumbered), a second set of column address diodes [124] (column 10, line 27) connected to a second set of address lines (unnumbered), and a resistive element [112] connected between the first set of address lines and a pull up voltage +V (column 10, line 19), and a resistive element [122] connected between the second set of address lines and a pull down voltage –V (column 10, line 25). Taussig et al. further disclosed resistors [112] and [122] are pull-up and pull down resistors (column 13, lines 50-51).

Regarding claim 12, Taussig et al. disclosed in Figure 10 a cross-point memory array [506] having a set of row electrodes [504] and a set of column electrodes [502], the row and column electrodes are orthogonal with each other, and diodes are formed at the intersections of the electrodes to create cross-point memory cell array [506] (column 13, lines 37-42), a first set of diodes (unnumbered} connected between a first set of row address lines [514], a second set of diodes (unnumbered) connected between a second set of column address lines [510], a set of pull-up/pull-down resistors coupled between the row/column address lines [514/510] and the row/column electrodes [504/502] (column 13, lines 47-53).

Regarding claim 2, Taussig et al disclosed in Figure 5 a unit cell of the memory array which would be used as the cross-point resistive element in the addressing circuit. The unit cell comprises two layers of orthogonal sets of spaced parallel conductors arranged with a semiconductor layer between (column 8, lines 65-67).

Regarding claim 3, Taussig et al. disclosed in Figure 7 the memory element [102] includes a fuse and a diode in series (column 10, lines 13-14), wherein the fuse is coupled to the row electrode [104] and the pull-up transistor [112], and the diode coupled to the column electrode and the pull-down transistor [122].

Regarding claim 4, Taussig et al. disclosed both the memory array and the addressing circuit to be fabricated using the same simple process (column 16, lines 9-10).

Regarding claims 8-9, 13 and 25, Taussig et al. disclosed in Figure 10 a row sense line [516] and a column sense line [512], each sense line connected to a plurality of diodes (unnumbered) (column 13, lines 67 and 53).

Regarding claim 19, Taussig et al. disclosed in Figure 3 a memory module [20] including a plurality of layer [22], each of the layers [22] comprises a memory array [25] and an addressing circuit [30] (column 7, lines 22-25).

Regarding claim 20, Taussig et al. disclosed how a memory element [262] is addressed and read (column 12, line 64 to column 13, line 14).

Regarding claims 22, 27, Taussig et al. showed in Figure 9, each of sense lines [274] and [284] includes a sense diodes [272] and [282] (column 12, line 55, 58-59).

5. Claims 5-7, 10-11, 14-18, 21, 23-24, 26, 28-29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Taussig et al. failed to show or suggest the resistive elements, the pull-up, pull-down resistive elements and the cross-point resistive elements in the memory elements having substantially the same temperature coefficient of resistivity as in claim 5, 16; or formed from substantially the same materials or fabrication process as in claim 6, 15, 23, 28; or the resistance of the pull-up, pull-down resistive elements as in claims 7, 17, 24, 29; or the resistive elements includes diodes as in claims 10, 18; or how the anodes and cathodes of the resistive elements coupled to the output/input of the pull-up/pull-down resistive elements as in claim 11; or how the resistive elements share the same conductive layer as in claim 14; or the step of applying a predetermined electrical signal to the at least one sense line for enabling or preventing writing to the addressed memory element as in claims 21, 26.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Taussig et al. is cited to show an addressing and sensing circuit for a cross-point diode memory array.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan T. Nguyen whose telephone number is (571) 272-

1789. The examiner can normally be reached on Monday to Friday from 07:00 AM to 03:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho, can be reached at (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tan T. Nguyen
Primary Examiner
Art Unit 2827
June 22, 2005